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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/078,441	02/21/2002	Naoshi Matsuo	1359.1062	4915

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EXAMINER	
HAROLD, JEFFEREY F	

ART UNIT	PAPER NUMBER
2644	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/078,441	MATSUO, NAOSHI	
	Examiner	Art Unit	
	Jefferey F Harold	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 21* is/are rejected.

7)☒ Claim(s) *18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Terminal Disclaimer

1. The terminal disclaimer filed on September 7, 2004 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of United States Patent 6,317,501 and United States Patent Application numbers 10/003,768, 10/035,507 and 10/038,188 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. ***Claims 1-17 and 21*** are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshida et al. (United States Patent 6,404,886), hereinafter referenced as Yoshida.

Regarding **claim 1**, Yoshida discloses a method and apparatus for echo canceling with multiple microphones. In addition, Yoshida discloses an echo cancellation processing system comprising in a full duplex telephony system: a microphone array; a loudspeaker for converting a speech signal transmitted from a telephony system on a communication partner side to a speech; and an echo

cancellation processing part comprising an estimated wraparound speech signal generating part for estimating a speech signal that is outputted from the loudspeaker and wraps around to the microphone array, using a time difference between input speech signals of a plurality of channels of the microphone array, and generate an estimated wraparound speech signal in accordance with an estimated result based on an output speech signal supplied to the loudspeaker, and a subtracter for subtracting the estimated wraparound speech signal from an input speech signal inputted to the microphone array, as disclosed at column 3, line 44 through column 8, line 20 and exhibited in figure 2-9.

Regarding **claim 2**, Yoshida discloses everything claimed as applied above (see claim 1), in addition, Yoshida discloses a wraparound delay amount detecting part for comparing an output speech signal supplied to the loudspeaker with a wraparound speech signal contained in an input speech signal inputted though the microphone array, and detecting a delay amount of the wraparound speech signal contained in the input speech signal delayed from the output speech signal; and a delay processing part for delaying the output speech signal in accordance with the delay amount detected by the wraparound delay amount detecting part, wherein an output speech signal of the delay processing part is inputted to the estimated wraparound speech signal generating part as an input signal, as disclosed at column 3, line 44 through column 8, line 20 and exhibited in figure 2-9.

Regarding **claim 3**, Yoshida discloses everything claimed as applied above (see claim 2), in addition, Yoshida discloses a wraparound speech signal emphasizing part

for emphasizing and extracting the wraparound speech signal from the input speech signal, wherein the wraparound speech signal emphasizing part comprises: a first delay amount calculating part for calculating a delay amount between the respective microphone input signals delayed from the loudspeaker based on input speech signals inputted through each microphone constituting the microphone array; and a first addition processing part for conducting synchronous addition processing regarding an input speech signal inputted through each microphone constituting the microphone may, by adjusting the delay amount between the respective microphone input signals delayed from the loudspeaker, and emphasizing the wraparound speech signal, and the emphasized wraparound speech signal is inputted to the wraparound delay amount detecting part, as disclosed at column 3, line 44 through column 8, line 20 and exhibited in figure 2-9.

Regarding **claim 4**, Yoshida discloses everything claimed as applied above (see claim 3), in addition, Yoshida discloses wherein the first addition processing part comprises: a delay unit for adjusting the delay amount between the respective microphone input signals delayed from the loudspeaker corresponding to each microphone constituting the microphone array; and an adder whose input signal is an output signal of the delay unit through each microphone, as disclosed at column 3, line 44 through column 8, line 20 and exhibited in figure 2-9.

Regarding **claim 5**, Yoshida discloses everything claimed as applied above (see claim 4), in addition, Yoshida discloses a speaker's speech signal emphasizing part for conducting synchronous addition processing of a speaker's speech signal inputted

through each microphone constituting the microphone array, and emphasizing the speaker's speech signal, thereby generating an input speech signal in which a speaker signal is emphasized, as disclosed at column 3, line 44 through column 8, line 20 and exhibited in figure 2-9.

Regarding **claim 6**, Yoshida discloses everything claimed as applied above (see claim 5), in addition, Yoshida discloses a second delay amount calculating part for calculating a delay amount between respective microphone input signals delayed from the speaker based on input speech signals inputted through each microphone constituting the microphone array; and a second addition processing part for executing synchronous addition processing regarding an input speech signal inputted through each microphone constituting the microphone array, by adjusting the delay amount between the respective microphone input signals delayed from the speaker, and emphasizing the speaker's speech signal, as disclosed at column 3, line 44 through column 8, line 20 and exhibited in figure 2-9.

Regarding **claim 7**, Yoshida discloses everything claimed as applied above (see claim 6), in addition, Yoshida discloses wherein the second addition processing part comprises: a delay unit for adjusting the delay amount between the microphone input signals delayed from the speaker corresponding to each microphone constituting the microphone array; and an adder whose input signal is an output signal of the delay unit through each microphone, as disclosed at column 3, line 44 through column 8, line 20 and exhibited in figure 2-9.

Regarding **claim 8**, Yoshida discloses everything claimed as applied above (see claim 3), in addition, Yoshida discloses a speaker's speech signal emphasizing part for conducting synchronous addition processing of a speaker's speech signal inputted through each microphone constituting the microphone array, and emphasizing the speaker's speech signal, thereby generating an input speech signal in which a speaker signal is emphasized, as disclosed at column 3, line 44 through column 8, line 20 and exhibited in figure 2-9.

Regarding **claim 9**, Yoshida discloses everything claimed as applied above (see claim 8), in addition Yoshida discloses, wherein the speaker's speech signal emphasizing part comprises: a second delay amount calculating part for calculating a delay amount between respective microphone input signals delayed from the speaker based on input speech signals inputted through each microphone constituting the microphone array; and a second addition processing part for executing synchronous addition processing regarding an input speech signal inputted through each microphone constituting the microphone may, by adjusting the delay amount between the respective microphone input signals delayed from the speaker, and emphasizing the speaker's speech signal, as disclosed at column 3, line 44 through column 8, line 20 and exhibited in figure 2-9.

Regarding **claim 10**, Yoshida discloses everything claimed as applied above (see claim 9), in addition, Yoshida discloses wherein the second addition processing part comprises: a delay unit for adjusting the delay amount between the microphone input signals delayed from the speaker corresponding to each microphone constituting

the microphone array; and an adder whose input signal is an output signal of the delay unit through each microphone, as disclosed at column 3, line 44 through column 8, line 20 and exhibited in figure 2-9.

Regarding **claim 11**, Yoshida discloses everything claimed as applied above (see claim 2), in addition, Yoshida discloses a speaker's speech signal emphasizing part for conducting synchronous addition processing of a speaker's speech signal inputted through each microphone constituting the microphone array, and emphasizing the speaker's speech signal, thereby generating an input speech signal in which a speaker signal is emphasized, as disclosed at column 3, line 44 through column 8, line 20 and exhibited in figure 2-9.

Regarding **claim 12**, Yoshida discloses everything claimed as applied above (see claim 11), in addition, Yoshida discloses wherein the speaker's speech signal emphasizing part comprises: a second delay amount calculating part for calculating a delay amount between respective microphone input signals delayed from the speaker based on input speech signals inputted through each microphone constituting the microphone array; and a second addition processing part for executing synchronous addition processing regarding an input speech signal inputted through each microphone constituting the microphone array, by adjusting the delay amount between the respective microphone input signals delayed from the speaker, and emphasizing the speaker's speech signal, as disclosed at column 3, line 44 through column 8, line 20 and exhibited in figure 2-9.

Regarding **claim 13**, Yoshida discloses everything claimed as applied above (see claim 12), in addition, Yoshida discloses wherein the second addition processing part comprises: a delay unit for adjusting the delay amount between the microphone input signals delayed from the speaker corresponding to each microphone constituting the microphone array; and an adder whose input signal is an output signal of the delay unit through each microphone, as disclosed at column 3, line 44 through column 8, line 20 and exhibited in figure 2-9.

Regarding **claim 14**, Yoshida discloses everything claimed as applied above (see claim 1), in addition, Yoshida discloses a speaker's speech signal emphasizing part for conducting synchronous addition processing of a speaker's speech signal inputted through each microphone constituting the microphone array, and emphasizing the speaker's speech signal, thereby generating an input speech signal in which a speaker signal is emphasized, as disclosed at column 3, line 44 through column 8, line 20 and exhibited in figure 2-9.

Regarding **claim 15**, Yoshida discloses everything claimed as applied above (see claim 14), in addition, Yoshida discloses wherein the speaker's speech signal emphasizing part comprises: a second delay amount calculating part for calculating a delay amount between respective microphone input signals delayed from the speaker based on input speech signals inputted through each microphone constituting the microphone array; and a second addition processing part for executing synchronous addition processing regarding all input speech signal inputted though each microphone constituting the microphone array, by adjusting the delay amount between the

respective microphone input signals delayed from the speaker, and emphasizing the speaker's speech signal, as disclosed at column 3, line 44 through column 8, line 20 and exhibited in figure 2-9.

Regarding **claim 16**, Yoshida discloses everything claimed as applied above (see claim 15), in addition, Yoshida discloses wherein the second addition processing part comprises: a delay unit for adjusting the delay amount between the microphone input signals delayed from the speaker corresponding to each microphone constituting the microphone array; and an adder whose input signal is an output signal of the delay unit through each microphone, as disclosed at column 3, line 44 through column 8, line 20 and exhibited in figure 2-9.

Regarding **claim 17**, Yoshida discloses everything claimed as applied above (see claim 1), in addition, Yoshida discloses wherein the estimated wraparound speech signal generating part comprises an adaptive filter, and a coefficient updating part for updating a coefficient of the adaptive filter at a predetermined timing, wherein the coefficient updating part determines the estimated result and a coefficient update amount of the adaptive filter based on a level of a wraparound speech signal remaining in an echo cancellation result obtained by the echo cancellation processing part, and the adaptive filter conducts the adaptation based on an output speech signal supplied to the loudspeaker and generates the estimated wraparound speech signal, as disclosed at column 3, line 44 through column 8, line 20 and exhibited in figure 2-9.

Regarding **claim 21**, it is interpreted and thus rejected for the reasons set forth above in the rejection of claims 1-17.

Allowable Subject Matter

3. ***Claims 18-20*** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jefferey F Harold whose telephone number is 571-272-7519. The examiner can normally be reached on Monday - Friday 9 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh H Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jefferey F Harold
Examiner
Art Unit 2644

JFH
April 1, 2005